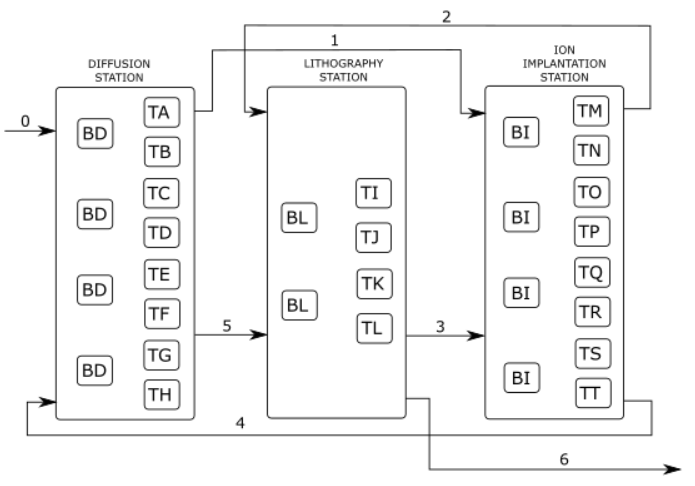
Case study  
  
Consider a scaled-up version of the Intel Mini-Fab [1], a benchmark model that has been used in various scheduling studies for wafer fabs [2,3]. The Mini-Fab model has been scaled-up by a factor of four to construct a scheduling example with more available choices for production scheduling. The scaled-up Mini-Fab has three stations: diffusion, lithography, and ion implantation, where wafer lots of types Pa and Pb are fabricated. The general flow of the wafer lots, shown in Figure 01, is the same for both product types:

Start >> Diffusion (S1) >> Ion implantation (S2) >> Lithography (S3) >> Ion implantation (S4) >> Diffusion (S5) >> Lithography (S6) >> Exit



**Figure 01.** Diagram of process flow in scaled-up Mini-Fab.

Equipment for all stations is also shown in Figure 01. Tools are assigned to processing steps S1 to S6 as described in Table 1. Equipment preemption is not allowed so once a tool begins the execution of a step, the step must be completed. Loading and unloading times are neglected. Every station is equipped with buffers (BD, BL, and BI) but their capacity is assumed infinite.

**Table 1.** Processing step – equipment – processing time mapping

|  |  |  |  |
| --- | --- | --- | --- |
| Equipment | Processing step | Pa and Pb | |
| TA - TH | S1 & S5 | S1 = 225 min | S5 = 255 min |
| TI - TL | S2 & S4 | S2 = 30 min | S4 = 50 min |
| TM - TT | S3 & S6 | S3 = 55 min | S6 = 10 min |

The fab uses dynamic scheduling/dispatching where wafer lots are matched with tools by solving a dynamic integer programming problem [4]. Wafer lots are assigned to tools based on the cost *c* of tools *j* at time *t,* defined in equation (1). The cost of a tool is a weighted sum of *fij*, where *i* denotes the factor and *j* the tool. Factors in equation (1) may correspond to the recommended factors for scheduling applications identified by SEMATECH: downtime, setup, yield, and dispatch rule [5]. Weights *wi* are normalized to facilitate the addition or removal of factors.

 (1)

In the extended Mini-Fab example, Pb is a high-value wafer type where scrap results in a large loss (see Table 2). Such large losses may be prevented by incorporating tool capability in scheduling to ensure that high-value lots are matched with high-capability tools. Tool capability is quantified with the process capability index (Cpk), estimated in a lot-by-lot manner for every tool in the fab. Six sigma conversion tables are used to relate the Cpk of tools in the fab to estimated yield in Table 3 [6].

**Table 2.** Revenue and scrap loss for wafer lot types.

|  |  |  |
| --- | --- | --- |
|  | Revenue (US $) | Scrap loss (US $) |
| Pa | 1000 | -200 |
| Pb | 5000 | -1000 |

**Table 3.** Equipment capability and estimated yield [Need to find reasonable values]

|  |  |  |
| --- | --- | --- |
|  | Estimated yield | Cpk |
| TA |  |  |
| TB |  |  |
| TC |  |  |
| TD |  |  |
| TE |  |  |
| TF |  |  |
| TG |  |  |
| TH |  |  |
| TI |  |  |
| TJ |  |  |
| TK |  |  |
| TM |  |  |
| TL |  |  |
| TO |  |  |
| TP |  |  |
| TQ |  |  |

Cpk estimates can be incorporated in equation (1) to promote the use of more capable tools for high-value lots and minimizing scrap loss. For example, the cost of candidate tools can be defined as:

 (2)







[Show simulation results of capability-aware scheduling here – Describe how the weights are chosen]

The dynamic scheduling/dispatching method illustrated in Figures XX covers only lot-to-equipment assignments, which are often made with a tool-centric view. In practice, lot-to-equipment push rules would benefit from more information about the upcoming lots. For example:  
a) Information about the route followed by each lot and the current processing step would allow matching more-mature, high-cost lots with high capability tools. The rationale for this modifications comes from the fact that yield becomes increasingly important as the lot matures because of all of the value that has been added to the lot in the previous processing stages.

b) It is preferable to assign several lots of the same type to the same equipment because setup time decreases, and it benefits APC by providing better data for lot-to-lot (L2L) control.

Improving lot-to-equipment (“push”) assignments would require information from the lots running in the fab, which could be obtained from a global view of the fab. As described in section XX, the proposed approach can be followed to incorporate recommendations made by factory-wide analyses. Let us consider the case in which we would like to give preference to more-mature, high-value lots. In this case, it would be sufficient to change the structure of factor *f2* so that the new factor takes into account the maturity of the wafer lot



where n indicates the current operational step and N is the total number of steps for the lot.

The possibility of incorporating information about the route followed by the lots, as provided by the global view of the fab, goes far beyond the example illustrated herein. The dynamic scheduling approach may be used to aid with “training” (sequencing wafer lots of the same kind), or with predictive scheduling. The general form of the integer programming problem would remain the same and it would only differ on the factors used to construct the cost function (1).

[Show simulation results of capability-aware scheduling with recommendations from fab-wide analysis here]

References

[1] Kempf, K. (1994). Intel five-machine six step mini-fab description. Intel/ASU Report, Arizona State University.

[2] Vargas-Villamil, F. D., Rivera, D. E., & Kempf, K. G. (2003). A hierarchical approach to production control of reentrant semiconductor manufacturing lines. IEEE Transactions on control systems technology, 11(4), 578-587.

[3] Yoon, H. J., & Shen, W. (2008). A multiagent-based decision-making system for semiconductor wafer fabrication with hard temporal constraints. IEEE Transactions on Semiconductor Manufacturing, 21(1), 83-91.

[4] Pinedo, M. (2012). Scheduling. New York: Springer.

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